L Number	Hits	Search Text	DB	Time stamp
1	1910493	chip die semiconductor (integrated adj circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/12 19:13
2	285182	(chip die semiconductor (integrated adj circuit)) and (leadframe lead)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/12 19:20
3	54968	((chip die semiconductor (integrated adj circuit)) and (leadframe lead)) and (paddle ((chip die) adj4 attached pad))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/12 19:22
4	27644	(((chip die semiconductor (integrated adj circuit)) and (leadframe lead)) and (paddle ((chip die) adj4 attached pad))) and wires	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/12 19:22
5	5310	((((chip die semiconductor (integrated adj circuit)) and (leadframe lead)) and (paddle ((chip die) adj4 attached pad))) and wires) and (bond adj4 pad)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/12 19:22
6	200	(((((chip die semiconductor (integrated adj circuit)) and (leadframe lead)) and (paddle ((chip die) adj4 attached pad))) and wires) and (bond adj4 pad)) and (tie adj bar)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/12 19:24

DERWENT-ACC-NO: 1996-332300
DERWENT-WEEK: 199633

TITLE: Lead frame for multi-pin semiconductor quad flat package - has ring pad
located between die pad and inner lead, and supported by tie bar, with ring pad
having bonding pad attached to it

INVENTOR: KIM, K; PARK, B

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 1991KR-0019690 (November 6, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 9408340 B1	September 12, 1994	N/A	001	H01L 023/495

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR 9408340B1	N/A	1991KR-0019690	November 6, 1991

INT-CL (IPC): H01L023/495

ABSTRACTED-PUB-NO: KR 9408340B
BASIC-ABSTRACT: The lead frame of the multi-pin quad flat package (QFP) has the
ring pad (36) located between the die pad (32) and the inner lead (31), and
supported by the tie bar (33). The ring pad has the bonding pad (37) attached
to it and is used for double-wire bonding between an electrode pad (39) and an
inner lead (31).

ADVANTAGE - Lowers defects like wire declining, short, or disconnection.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS:
LEAD FRAME MULTI PIN SEMICONDUCTOR QUAD FLAT PACKAGE RING PAD LOCATE DIE PAD
INNER LEAD SUPPORT TIE BAR RING PAD BOND PAD ATTACH

DERWENT-CLASS: U11

EPI-CODES: U11-D01A1; U11-D03A1A;

DERWENT-ACC-NO: 1996-332300

DERWENT-WEEK: 199633

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
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APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
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INT-CL (IPC): H01L023/495

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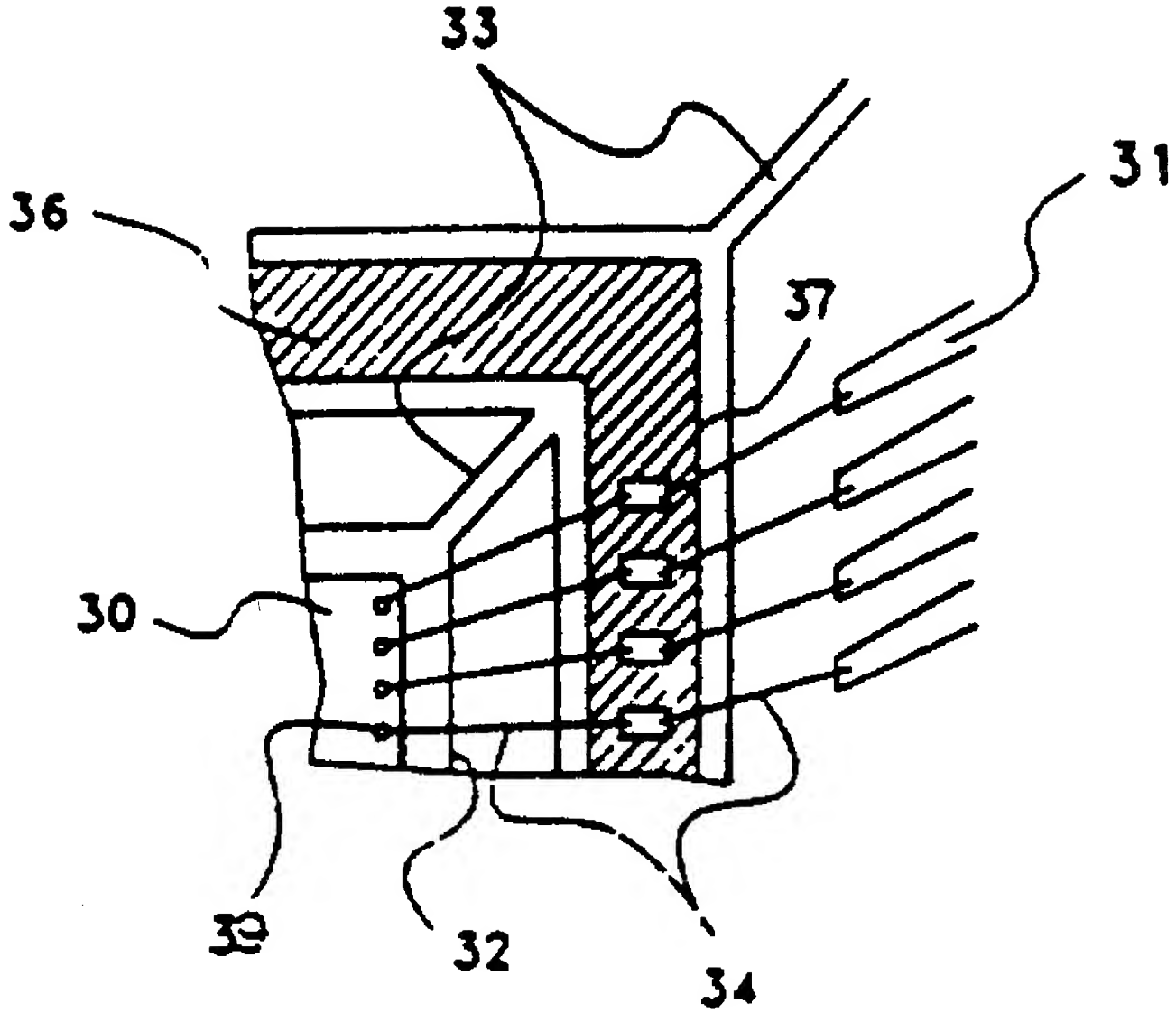
CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: LEAD FRAME MULTI PIN SEMICONDUCTOR QUAD FLAT PACKAGE RING PAD LOCATE DIE PAD INNER LEAD SUPPORT TIE BAR RING PAD BOND PAD ATTACH

DERWENT-CLASS: U11

EPI-CODES: U11-D01A1; U11-D03A1A;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